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(54) Bypassing pixel clock generation and CRTC circuits in a graphics controller chip

(57) In a video processor unit, a method of providing a video data stream at a clock rate that is independent of a pixel clock rate. Receiving native video data from a video source at a native clock rate, storing the video data in a memory unit, reading selected portions of the video data at a memory clock rate, rasterizing the selected video data, packetizing the rasterized video data, sending the packetized video data to a display unit by way of a link at a link rate, wherein the link rate is directly related to the memory clock rate.

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Description

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This patent application takes priority under 35 U.S.C. 119(e) to (i) U.S. Provisional Patent Application No.: 60/504,060 (Attorney Docket No. GENSP013P2) filed on September 18,2003, entitled "DIGITAL/ANALOG VIDEO INTERCONNECT AND METHODS OF USE THEREOF" by Kobayashi, and (ii) U.S. Provisional Patent Application No.: 60/562,737 (Attorney Docket No. GENSP113P) filed on April 15, 2004, entitled "BYPASSING PIXEL CLOCK GENEARATION AND CRTC CIRCUITS IN A GRAPHICS CONTROLLER CHIP" by Kobayashi each of which are hereby incorporated by reference herein in their entirety. This application is also related to the following co-pending U.S. Patent applications each of which are incorporated by reference, (i) U. S. Patent Application No. 10/726,802 (Attorney Docket No.: GENSP014), entitled "METHOD OF ADAPTIVELY CONNECTING A VIDEO SOURCE AND A VIDEO DISPLAY" naming Kobayashi as inventor; (ii) U.S. Patent Application No. 10/726,438 (Attorney Docket No.: GENSP015), entitled "METHOD AND APPARATUS FOR EFFICIENT TRANSMISSION OF MULTIMEDIA DATA PACKETS" naming Kobayashi as inventor; (iii) U. S. Patent Application No. 10/726,440, (Attorney Docket No.: GENSP105), entitled "METHOD OF OPTIMIZING MULTIMEDIA PACKET TRANSMISSION RATE", naming Kobayashi as inventor; (iv) U.S. Patent Application No. 10/727,131 (Attorney Docket No.: GENSP104), entitled "USING AN AUXILARY CHANNEL FOR VIDEO MONITOR TRAINING", naming Kobayashi as inventor; (v) U.S. Patent Application No. 10/726,350 (Attorney Docket No.: GENSP 106), entitled "TECHNIQUES FOR REDUCING MULTIMEDIA DATA PACKET OVERHEAD", naming Kobayashi as inventor; (vi) U.S. Patent Application No. 10/726,362 (Attorney Docket No.: GENSP107), entitled "PACKET BASED CLOSED LOOP VIDEO DISPLAY INTERFACE WITH PERIODIC STATUS CHECKS", naming Kobayashi as inventor; (vii) U.S. Patent Application No. 10/726,895 (Attorney Docket No.: GENSP108), entitled "MINIMIZING BUFFER REQUIREMENTS IN A DIGITAL VIDEO SYSTEM", naming Kobayashi as inventor; and (viii) U.S. Patent Application No. 10/726,441 (Attorney Docket No.: GENSP109), entitled "VIDEO INTERFACE ARRANGED TO PROVIDE PIXEL DATA INDEPENDENT OF A LINK CHARACTER CLOCK", naming Kobayashi as inventor; (ix) U.S. Patent Application No. 10/726,934 (Attorney Docket No.: GENSP110), entitled "ENUMERATION METHOD FOR THE LINK CLOCK RATE AND THE PIXEL/AUDIO CLOCK RATE", naming Kobayashi as inventor, and (x) U.S. Patent Application No. 10/726,794 (Attorney Docket No.: GENSP013), entitled "PACKET BASED VIDEO DISPLAY INTERFACE AND METHODS OF USE THEREOF" naming Kobayashi as inventor. BACKGROUND

I. FIELD OF THE INVENTION

[0002] The invention relates to display devices. More specifically, the invention describes a method and apparatus for using driving LCD panel drive electronics.

OVERVIEW

[0003] Until most recently, almost all TVs in use today rely on a device known as the cathode ray tube, or CRT, to display their images. In order to display an image on the entire screen, electronic circuits inside the TV use magnetic deflection coils (a horizontal deflection coil to move the beam from left to right and a vertical deflection coil to move the beam up and down) to move the electron beam in a "raster scan" pattern across and down the screen. Fig. 1 illustrates a raster 100 on a conventional cathode ray tube where an electron beam paints one line across the screen from left to right 102a and then quickly moves back to the left side 104, and paints another horizontal line 102b, while continuously moving down slightly. When the beam reaches the right side of the bottom line 107, it is moved back to the upper left comer of the screen, as represented by line 106. When the beam is "painting" lines 102 it is on, and when it is "retracing" lines 104, it is off so that it does not leave a trail on the screen. The term horizontal retrace is used to refer to the beam moving back to the left at the end of each line, while the term vertical retrace refers to its movement from the bottom to the top of the raster 106.

[0004] In order to display an image on a CRT display screen, each image is transmitted as a sequence of frames each of which includes a number of horizontal scan lines. Typically, time reference signals are provided in order to divide the video signal into horizontal scan lines and frames. These reference signals include a VSYNC signal that indicates the beginning of a frame and an HSYNC signal that indicates the beginning of a next source scan line. In this way, the image is divided into a number of points where each point is displayed as a pixel having a corresponding pixel clock that specifies the rate at which pixels are generated (in pixels per second). Therefore, in order to display video data from a video source, such as a CPU, DVD player, etc., the video data is processed by a conventional video processor unit (VPU) that converts the incoming video data (at a native format) to a video data at a video display format at a clock rate determined by a memory unit into which the data is temporarily stored.

[0005] A cathode ray tube (CRT) controller unit then converts the display formatted video data to CRT compatible display timing by adding timing and control signals (such Hsync and Vsync) regardless of the whether or not the display unit is a cathode ray tube based display or a fixed pixel display such as an LCD. In this way, the CRT controller unit converts the video data that is read from the video source to a pixel clock rate Φ_{pixel} based solely upon the assumption that the display re-

quires CRT type signals. It should be noted therefore, that strictly based upon CRT legacy considerations, the incoming video signal has been converted from a native video clock Φ_{native} to a pixel clock Φ_{pixel} and then sent to the display unit at a link rate LR that must be faster than the pixel clock Φ_{pixel}. At the display, the video signal must then be processed again by a pixel clock regenerator circuit in order for the video data to be properly displayed.

[0006] Therefore, even in those situations where a pixel clock rate is not meaningful (such as with fixed pixel displays, such as LCDs), conventional video processors require that a CRT controller unit force a video signal that will not be displayed on a CRT type display to conform to legacy CRT requirements.

[0007] Therefore, in those cases where a display is not CRT based, a video processor that does not enforce CRT legacy requirements is desirable.

SUMMARY OF THE INVENTION

[0008] What is provided is a video processor architecture embodied as a method, apparatus, and system suitable for implementation with digital displays, such as liquid crystal displays (LCDs), that provides a video signal that is directly related to a memory clock rate and independent of a pixel rate.

[0009] In a video processor unit, a method of providing a video data stream at a clock rate that is independent of a pixel clock rate. Receiving native video data from a video source at a native clock rate, storing the video data in a memory unit, reading selected portions of the video data at a memory clock rate, rasterizing the selected video data, packetizing the rasterized video data, sending the packetized video data to a display unit by way of a link at a link rate, wherein the link rate is directly related to the memory clock rate.

[0010] In another embodiment, a video processor for displaying video data on a non-CRT type display unit coupled thereto by way of a link is disclosed that includes a video memory unit having an associated memory clock rate and a video packet transmitter unit for transmitting the video data to the non-CRT type display in the form of video data packets at a link rate that is directly related to the memory clock rate Φ_{memory} such that the video processor does not require a CRT controller unit.

[0011] In still another embodiment, a configurable video processor for providing displayable video data to a display unit coupled thereto is disclosed. The video processor includes a CRTC circuit, a selectable CRT controller circuit coupled to the CRTC circuit and a raster engine coupled to the selectable CRT controller circuit. The processor also includes a display interrogator unit coupled to the display unit and the selectable CRT controller circuit for determining a display type corresponding to the display unit, wherein when the display type is a non-CRT type display, the display interrogator unit sends a first signal to the selectable CRT controller circuit that disables (if enabled) the CRTC circuit such that the displayable video data is sent directly to the display unit from the raster engine and wherein when the display interrogator determines that the display is a CRT type display, then the display interrogator sends a second signal to the selectable CRT controller circuit that enables the CRTC circuit (if disabled) such that the displayable video data is processed by the CRTC circuit prior to being sent to the display unit by way of the link.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012]

FIG. 1 illustrates a raster on a conventional cathode ray tube.

FIG. 2 shows an exemplary video processor unit (VPU) in accordance with an embodiment of the invention.

Fig. 3 shows an exemplary LCD display suitable for use with the VPU shown in FIG. 3.

FIG. 4 shows a high-level diagram of a data stream for transmission over the link in accordance with an embodiment of the invention.

FIG. 5 illustrates a system that can be used to implement the invention.

DETAILED DESCRIPTION OF SELECTED EMBODIMENTS

[0013] Reference will now be made in detail to a particular embodiment of the invention an example of which is illustrated in the accompanying drawings. While the invention will be described in conjunction with the particular embodiment, it will be understood that it is not intended to limit the invention to the described embodiment. To the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

[0014] Until most recently, almost all TVs in use today rely on a device known as the cathode ray tube, or CRT, to display their images. In order to display an image on the entire screen, electronic circuits inside the TV use magnetic deflection coils (a horizontal deflection coil to move the beam from left to right and a vertical deflection coil to move the beam up and down) to move the electron beam in a "raster scan" pattern across and down the screen. In order to display video data from a video source, such as a CPU, DVD player, etc., the video data provided by a video source at a native clock rate Φ_{native} is processed by a conventional video processor unit (VPU) by storing the video data in a video memory unit until such time as it is read from the memory at a memory clock rate Φ_{memory} and processed by a raster engine that converts the video data native format to a video signal having a displayable format based upon the charac-

teristics of the display unit for which the image will be displayed..

[0015] A cathode ray tube (CRT) controller unit then converts the video signal using display timing by adding timing and control signals (such Hsync and Vsync) regardless of the whether or not the display unit is a cathode ray tube based display or a fixed pixel display such as an LCD. In this way, the CRT controller unit converts the video data that is read from the memory unit at the memory clock rate Φ_{memory} to a pixel clock rate Φ_{pixel} based solely upon the assumption that the display requires CRT type signals. Once the CRT controller unit has added the CRT based control and timing signals, the video signal is then passed by way of a link to the display unit at a link rate LR. Therefore, even in those situations where a pixel clock rate is not meaningful (such as with fixed pixel displays, such as LCDs), conventional video processors require that a CRT controller unit force a video signal that will not be displayed on a CRT type display to conform to legacy CRT requirements.

[0016] Accordingly, the invention describes a method, system, and apparatus that does not enforce CRT legacy requirements for those situations where a video is to be displayed on a non-CRT type display unit, such as an LCD. More specifically, the inventive video processor does not force the video signal to conform to a pixel clock but preserves the memory clock rate by transmitting the video data in video data packets at a link rate that is directly related to the memory clock rate. In this way, the inventive video processor does not require a CRT controller unit for those situations where a display unit so connected is not a CRT type display. In some embodiments, the inventive processor is dedicated to a fixed pixel display and therefore does away with the CRT controller and associated circuitry entirely whereas in other embodiments, in order to maintain compatibility with all possible display environments, a selectable CRT controller circuit is included. The selection (or de-selection) of the CRT controller and associated circuitry is based upon a query of the display attributes during an initialization process whereby the video processor queries the display whether or not it is a CRT type display.

[0017] The invention will now be described in terms of a representative LCD panel. However, it should be noted that any digital fixed pixel display, be it LCD, plasma, DLP based, is also suitable and therefore the use of an LCD panel in the following description should not be considered to limit either the scope or the intent of the invention. It should be noted that the invention is also well suited to be used in conjunction with any packet based video display interface such as described in copending U.S. Patent Application Serial No.10/726,794 entitled "PACKET BASED VIDEO DISPLAY INTERFACE AND METHODS OF USE THEREOF" by Kobayashi filed December 3, 2003 and U.S. Patent Application Serial No. _____ entitled "USING PACKET TRANSFER FOR DRIVING LCD PANEL DRIVER ELECTRONICS" by Kobayashi filed concurrently with this application each of which are incorporated herein by reference for all purposes.

[0018] Accordingly, FIG. 2 shows an exemplary video processor unit (VPU) 200 in accordance with an embodiment of the invention. The VPU 200 includes an interface 202 coupled to a video source (not shown) such as a CPU, DVD player, etc. capable of providing a video signal V_1 at a native clock rate Φ_{native} and a native video format. It should be noted that the video source can include either or both a digital image (i.e. still or digital video) source and/or an analog image (i.e., still or analog video) source. Accordingly, the video source provides various video signals that can have any number and type of well-known formats, such as composite video, serial digital, parallel digital, RGB, or consumer digital video. The video signal can be an analog video signal provided the source includes some form of an analog video source such as for example, an analog television, still camera, analog VCR, DVD player, camcorder, laser disk player, TV tuner, set top box (with satellite DSS or cable signal) and the like. The source can also include a digital image source such as for example a digital television (DTV), digital still camera, and the like. The digital video signal can be any number and type of well known digital formats such as, SMPTE 274M-1995 (1920 x 1080 resolution, progressive or interlaced scan), SMPTE 296M-1997 (1280 x 720 resolution, progressive scan), as well as standard 480 progressive scan video.

[0019] Once received, the video data V_1 is then stored (by way of a write/modify operation) in a video memory unit 204 coupled to the interface 202 at a memory space location corresponding to the video window being displayed. In most cases, the memory unit 204 is of a size sufficient to store at least a full frame of video data In order to display the video data stored in the memory unit 204, selected portions of the video data V_1 are read from the memory 204 at a memory clock rate Φ_{memory} and processed by a raster engine 206 that converts the video data native format to a video signal V_2 having a displayable format based upon the characteristics of a display unit 208. For example, if the native format is 8 bit video data and the display unit 208 requires 24 bit video data, then the raster engine 206 has the option of utilizing a color look up table (CLUT) 210 in the conversion process.

[0020] Once the video signal V_2 has been properly formatted for display on the display unit 208, a packetizer 212 packetizes the video signal V_2 into a number of data packets 214 in the form of a data stream 215. The data stream 215 is transmitted to the display 208 by way of a link 216 at a transmission rate referred to as a link rate LR that is independent of the native stream rate Φ_{native} of the video data but is, however, directly related to the memory clock rate Φ_{memory} (i.e., $LR = \alpha \times \Phi_{memory}$). In the described embodiment, the speed, or link rate, of the link 216 can be configured to

include a number of logical data channels (not shown) that can be adjusted to compensate for link conditions. For example, at 2.5 Gbps per channel, the link 216 can support SXGA 60Hz with a color depth of 18 bits per pixel over a single channel. It should be noted that a reduction in the number of channels reduces not only the cost of interconnect, but also reduces the power consumption which is an important consideration (and desirable) for power sensitive applications such as portable devices and the like. However, by increasing the number of channels to four, the link 216 can support WQSXGA (3200 x 2048 image resolution) with a color depth of 24-bits per pixel at 60Hz. or QSXGA (2560 x 2048) with a color depth of 18-bits per pixel at 60Hz, without data compression. Even at the lowest rate of 1.0 Gbps per channel, only two channels are required to support an uncompressed HDTV (i.e., 1080i or 720p) data stream.

[0021] It should be noted, however, that the bandwidth of the link 216 must be greater than the aggregate bandwidth of all data stream(s) being transmitted over the link 216. In this way, the data packets 214 are received by and appropriately processed by a properly configured display 208 an example of which is described below without the need to generate a pixel clock at either the VPU 200 or the display 208. In one embodiment, the VPU 200 can optionally include a switch coupled to a CRT controller unit that provides the necessary CRT control signals and timing only in those cases where the display is a legacy CRT type display. In this way, the VPU can be used for any type display.

[0022] Fig. 3 shows an exemplary LCD display 300 suitable for use with the VPU 200. Accordingly, the LCD display 300 includes an LCD panel 302 having a number of picture elements 304 (pixels) that are arranged in a matrix connected to a data driver 306 by way of a plurality of data lines 308 and a plurality of gate lines 310. In the described embodiment, these picture elements 304 take the form of a plurality of thin film transistors (TFTs) 312 that are connected between the data lines 308 and the gate lines 310. During operation, each of a number of data latches 314 into which video data is stored, outputs digital data signals to an associated digital to analog converter (DAC) 316 by way of the data lines 308. Concurrently, each of a number of logic circuits 318 included in a gate driver 320 outputs a predetermined scanning signal to the gate lines 310 in sequence at timings that are in sync with a horizontal synchronizing signal. In this way, the TFTs 312 are turned ON when the predetermined scanning signal is supplied to the gate lines 310 to transmit the analog data signals supplied by the DACs 316 by way of the data lines 408 that ultimately drive selected ones of the picture elements 304.

[0023] In order to transmit the video data, the VPU 200 forms the data stream 215 that includes a number of the data packets 214 which are then received and processed by a display interface 322. In the described embodiment, the data packets 214 are then forwarded to directly to the data latches 314 included in the column driver 306 in such a way that all the video data (in the form of pixel data) used for the display of a particular frame line n of the video frame is provided to the data latches 314 within a line period τ. Therefore, once each data latch 314 has appropriate pixel data stored therein, the data driver 306 drive appropriate ones of the TFTs 312 in the LCD array 302.

[0024] Fig. 4 shows a high-level diagram of a data stream 400 for transmission over the link 216 formed of a number of video data packets 402 and audio data packets 404 multiplexed into the single data stream 400. In this example the video data packets 402 are consistent with UXGA graphics 1280x720p video (Stream ID = 1) having an associated audio in the form of the audio packets 504 (Stream ID = 2). In this example, each frame line is formed of at least 1280 pixels (or 3840 subpixels) therefore requiring 3840 data latches be used to store a single frame line of video data within the line period τ. For example, in one embodiment, when the data stream 400 is received at the display interface 322, a group of 3840 data packets (as defined by corresponding packet headers 406) are stored in a memory that takes the form of a frame buffer or a line buffer. It should also be noted, however, that the memory can be bypassed or be absent altogether if a strictly pipelined architecture is desired.

[0025] FIG. 5 illustrates a system 500 that can be used to implement the invention. The system 500 is only an example of a graphics system in which the present invention can be implemented. System 500 includes central processing unit (CPU) 510, random access memory (RAM) 520, read only memory (ROM) 525, one or more peripherals 530, graphics controller 560, primary storage devices 540 and 550, and digital display unit 570. CPU 510 is also coupled to one or more input/output devices 590. Graphics controller 560 generates image data and corresponding reference signals, and provides both to digital display unit 570. The image data can be generated, for example, based on pixel data received from CPU 510 or from an external circuitry.

[0026] Although only a few embodiments of the present invention have been described, it should be understood that the present invention may be embodied in many other specific forms without departing from the spirit or the scope of the present invention. The present examples are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope of the appended claims along with their full scope of equivalents.

[0027] While this invention has been described in terms of a preferred embodiment, there are alterations, permutations, and equivalents that fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing both the process and apparatus of the present invention. It is therefore

intended that the invention be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

Claims

1. In a video processor unit, a method of providing a video data stream at a clock rate that is independent of a pixel clock rate, comprising:

   receiving native video data from a video source at a native clock rate;
   storing the video data in a memory unit;
   reading selected portions of the video data in a memory unit at a memory clock rate;
   rasterizing the selected video data;
   packetizing the rasterized video data into a number of video data packets;
   sending the packetized video data to a display unit by way of a link at a link rate that is directly related to the memory clock rate.

2. A method as recited in claim 1 wherein the memory device is a line buffer arranged to store at least a quantity of video data consistent with a single frame line.

3. A method as recited in claim 1, wherein each of the video data packets includes a packet header and a packet payload, wherein the packet header includes a packet ID and wherein the packet payload includes video data suitable for driving a corresponding pixel.

4. A method as recited in claim 1, wherein the rasterizer is coupled to a color look up table.

5. A video processor for displaying video data on a non-CRT type display unit coupled thereto by way of a link, comprising:

   a video memory unit having an associated memory clock rate;
   a video packet transmitter unit for transmitting the video data to the non-CRT type display in the form of video data packets at a link rate that is directly related to the memory clock rate Φ_{memory} such that the video processor does not require a CRT controller unit.

6. A video processor as recited in claim 5, wherein the non-CRT type display is an LCD type display.

7. A video processor as recited in claim 5, further comprising:

   an interface coupled to a video source arranged to provide a video signal V_1 at a native clock rate Φ_{native} and a native video format;
   a memory controller unit coupled to the interface and the video memory unit arranged to receive and then store the video data is then stored by way of a write/modify operation in the video memory unit at a memory space location corresponding to a video window being displayed; and
   a raster engine coupled to the memory controller wherein in order to display the video data stored in the memory unit, selected portions of the stored video data are read from the video memory by the memory controller by way of a read operation at the memory clock rate Φ_{memory} and passed to the raster engine that converts video signal V_1 at the native video format Φ_{native} to a video signal V_2 having a displayable format based upon the characteristics of the display unit.

8. A video processor as recited in claim 7, further comprising:

   a packetizer coupled to the raster engine arranged to packetize the video signal V_2 into the video data packets;
   a link interface coupling the packetizer to the link arranged to form the video data packets into a video data stream that is transmitted to the display by way of the link at a link rate LR that is independent of the native stream rate Φ_{native} wherein the link rate LR is directly related to the memory clock rate Φ_{memory}.

9. A video processor as recited in claim 8 wherein the link is configurable to include a number of adjustable logical data channels that can be adjusted to compensate for any of a number of link conditions.

10. A configurable video processor for providing displayable video data to a display unit coupled thereto, comprising:

    a CRTC circuit;
    a selectable CRT controller circuit coupled to the CRTC circuit;
    a raster engine coupled to the selectable CRT controller circuit; a display interrogator unit coupled to the display unit and the selectable CRT controller circuit for determining a display type corresponding to the display unit, wherein when the display type is a non-CRT type display, the display interrogator unit sends a first signal to the selectable CRT controller circuit that disables (if enabled) the CRTC circuit such that the displayable video data is sent directly

to the display unit from the raster engine and wherein when the display interrogator determines that the display is a CRT type display, then the display interrogator sends a second signal to the selectable CRT controller circuit that enables the CRTC circuit (if disabled) such that the displayable video data is processed by the CRTC circuit prior to being sent to the display unit by way of the link.

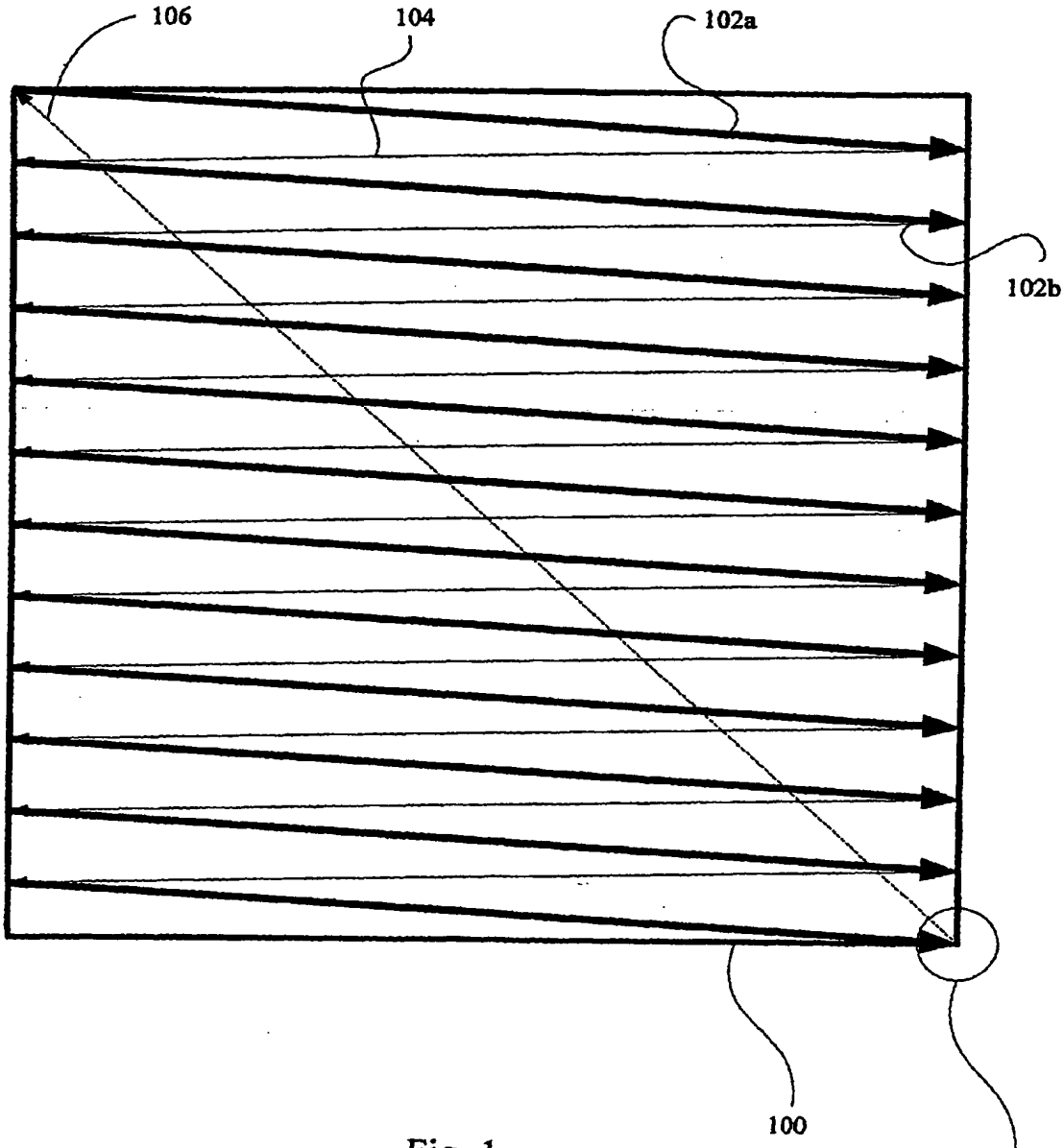


Fig. 1
Prior Art

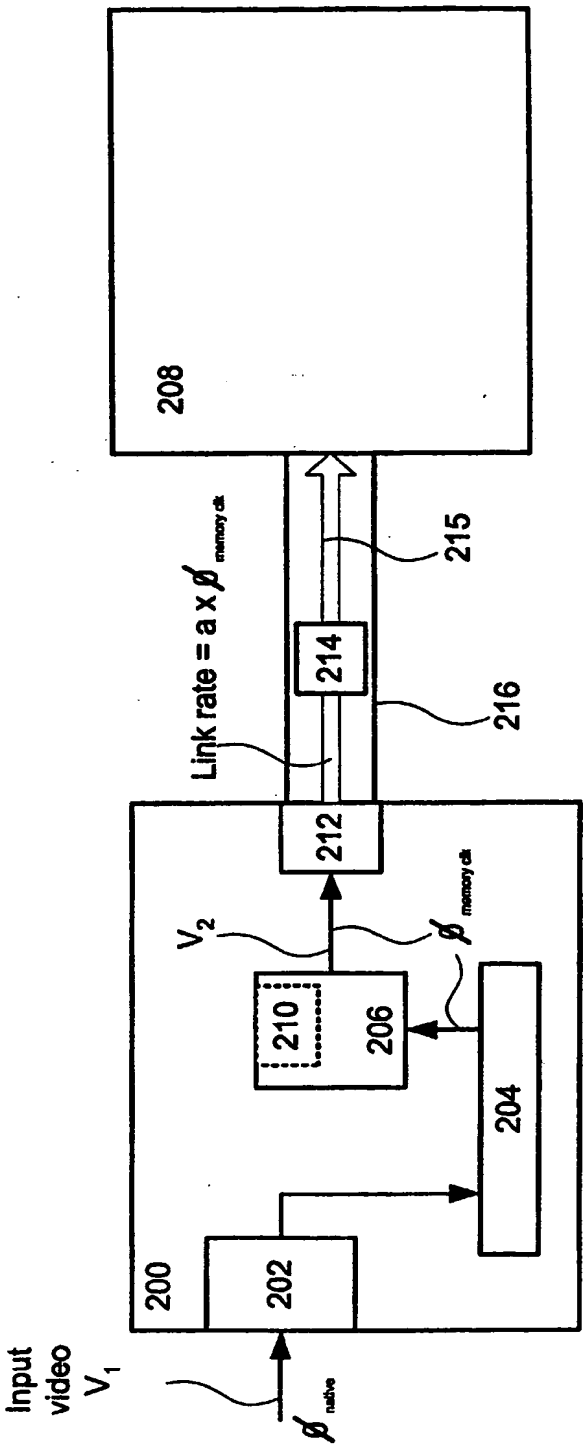
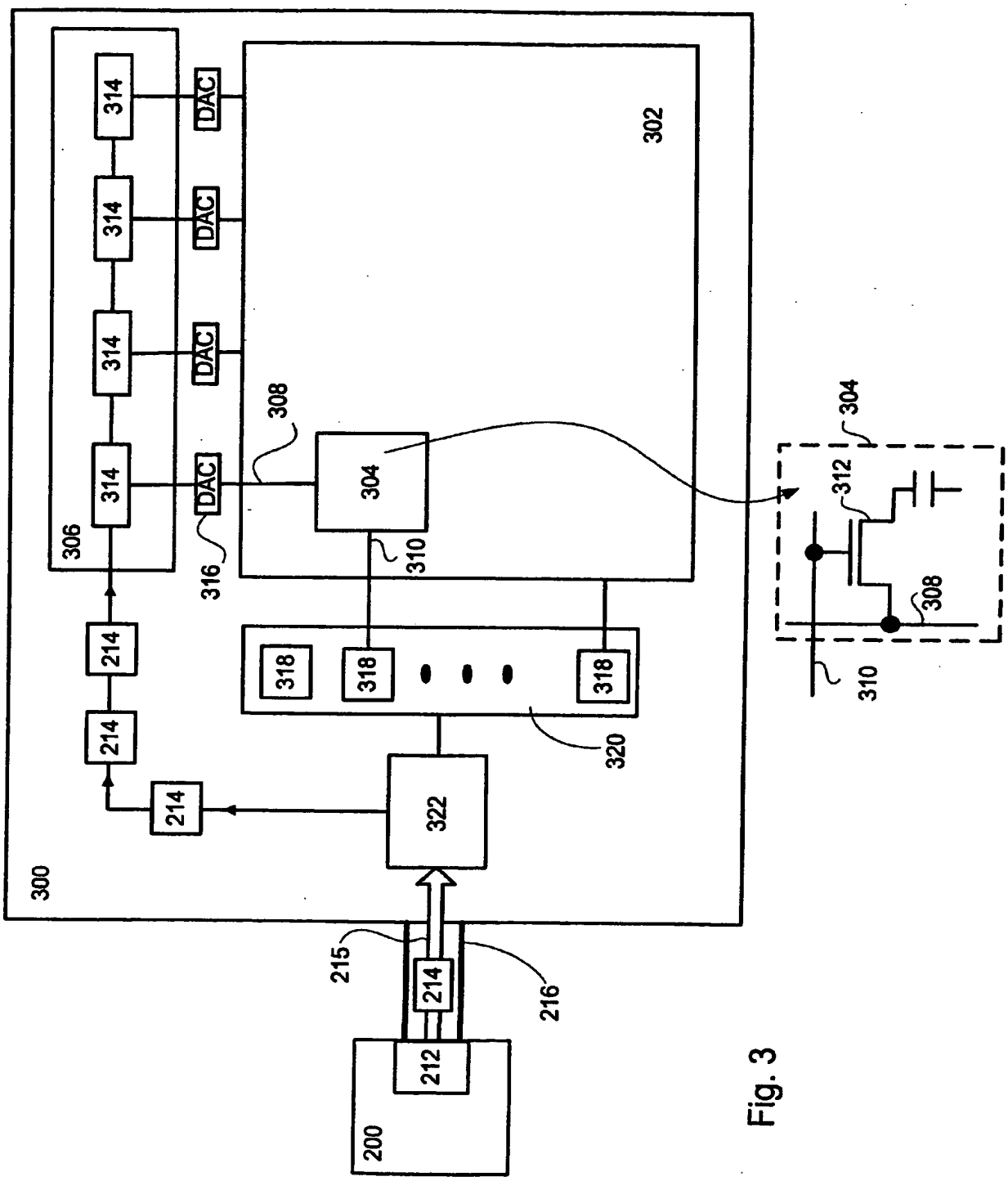

208
215
Link rate = a x $\phi'_{memory\ clk}$
214
216
212
V_2
$\phi_{memory\ clk}$
210
206
204
200
202
Input video V_1
ϕ_{native}

Fig. 2


300
302
304
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308
310
312
314
316
318
320
322
200
212
214
215
216
DAC

Fig. 3

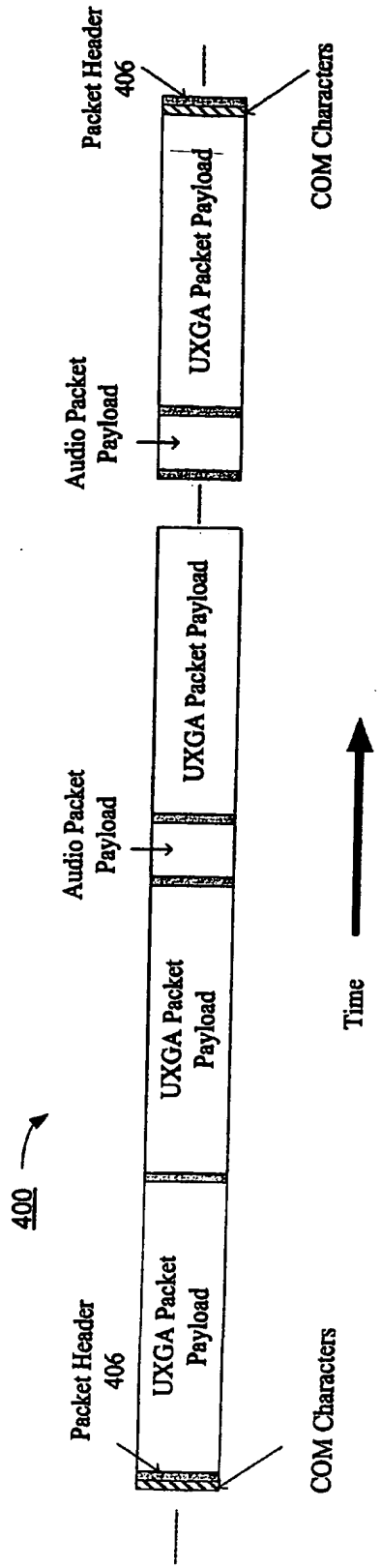
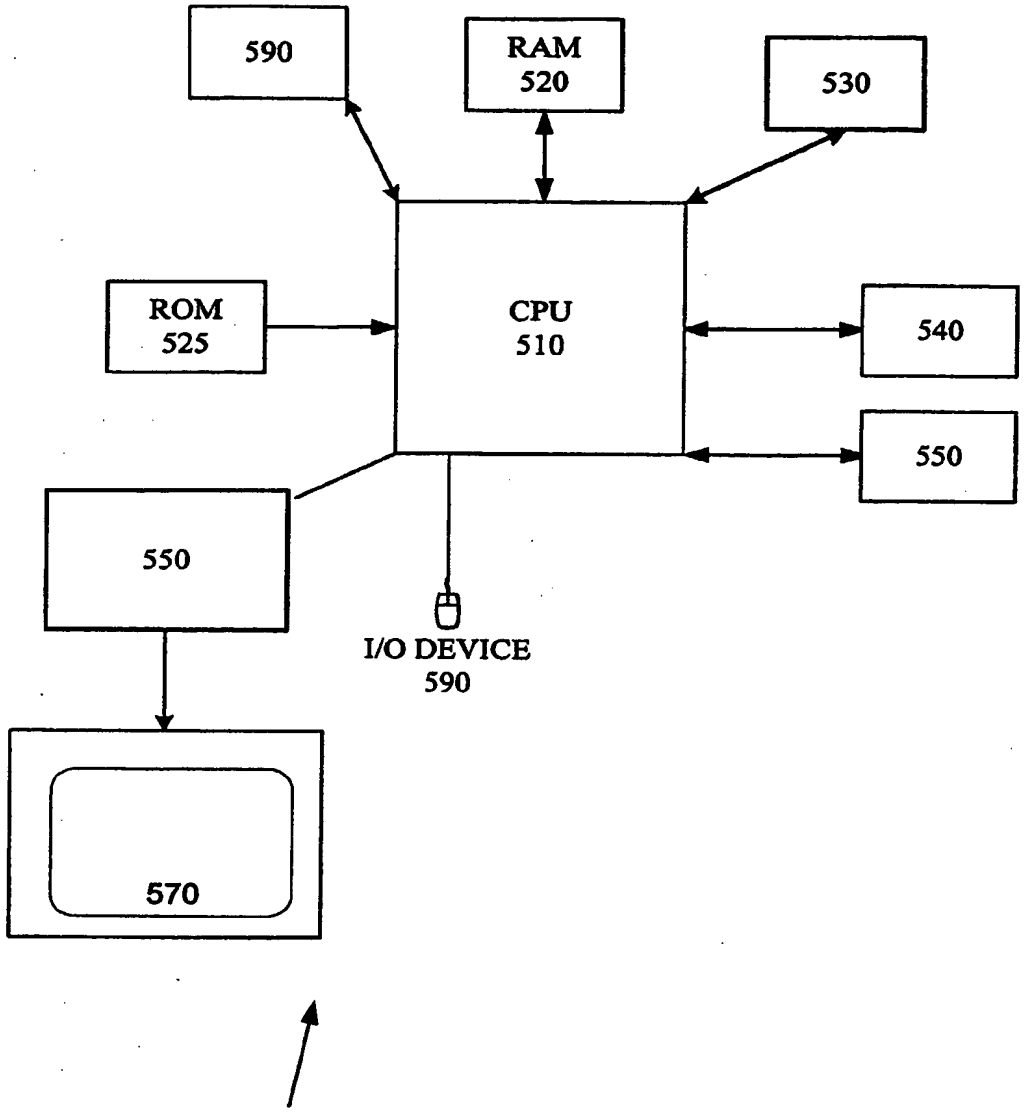


Fig. 4

High-level diagram of link traffic example


590
RAM
520
530
ROM
525
CPU
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I/O DEVICE
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Fig. 5